CMS32F0332 Datasheet

32-bit microcontrollers based on ARM® Cortex® -M0+

Rev. 0.5.5

Please note the following CMS IP policy

1. Features

1.1 MCU features

- **ARM Cortex™-M0+ core, 64MHz@2.1V~5.5V**
  - Single-cycle 32-bit hardware multiplier
- **32-bit hardware divider (DIVSQRT)**
  - Signed/unsigned mode, with 16 HCLKs to complete an operation
- **Memory**
  - Max. 64KB programmable FLASH (APROM+BOOT)
  - 1KB FLASH data area (seperated space)
  - Max. 8KB SRAM (with partition write protection function)
  - Support BOOT function, BOOT can be set to 0-4K
  - Support hardware CRC to check FLASH space codes
  - Support FLASH partition protection (min. unit: 2K)
- **System clock**
  - On-chip high-speed oscillation 48MHz/64MHz (HSI)
  - On-chip low-speed oscillation 40KHz (LSI)
- **GPIO (up to 30 I/Os)**
- **LVR (1.8V/2.0V/2.5V)**
- **LVD (2.0V/2.2V/2.4V/2.7V/3.0V/3.7V/4.0V/4.3V)**
- **System timer**
  - 24-bit SysTick timer
  - Watchdog timer (WDT)
  - Windowed watchdog timer (WWDT)
- **Normal mode/sleep mode/deep sleep mode**
- **Cyclic redundancy check (CRC)**
- **Timer (32bit/16bit-TIMER0/1/2/3)**
- **Capture/compare/pulse width modulation (CCP0/1)**
  - Support 4-channel simultaneous capture
- **Communication port**
  - 1x I^2C module (max. speed: 1Mb/s)
  - 1x SSP/SPI module (adjustable 4-16 bits data format)
  - Up to 2 UARTs: UART0/1 (total of 32
- **Enhanced PWM (EPWM)**
  - 6 channels and channels can be remapped
  - Support independent/complementary/synchronous/group output mode
  - Support edge/center alignment counting mode
  - Support one-shot/continuous/interval loading update mode
- **ADCA (12bit)**
  - Up to 31 input channels
  - Each conversion channel has an independent result register
  - Support one-shot/continuous mode
  - Support 2 hardware trigger modes and 9 trigger sources
  - 1 conversion result comparator which can generate interrupts
- **ADCB (12bit, 1.2Msps)**
  - Up to 31 input channels
  - Each conversion channel has an independent result register
  - Support one-shot/continuous/insert mode
  - Support external triggering method
  - 1 conversion result comparator which can generate interrupts
- **Analog comparator (ACMP0/1)**
  - 8 channels are selectable for positive side, internal 1.2V/VDD voltage for negative side
  - Support hysteresis voltage selection: 10mV/20mV/60mV
- **Programmable gain amplifier (PGA0/1)**
  - Positive 4-channel selection
  - Outputs can be connected to internal ADC channels with analog comparator inputs
  - Internal gain selection: 4x~32x
- **Operational amplifier (OP0/1)**
  - Inputs can be connected to internal 1.2V reference
  - Outputs can be connected to internal ADC

receive/transmit FIFOs) (TXD1 and RXD1 of UART1 can be assigned to any port)

- **Serial wire debug SWD (2-Wire)**
- **96bit unique ID (UID)**
- **128bit user UID (USRUID)**
  - Configurable by user, encryptable (can be used as a security key)

channels with analog comparator inputs
  - Can be set to comparator mode
- **Support safety-related functions and applications**
  - IEC60730 CLASS B standard qualified

1.2 Product comparison

Below is a product comparison of this family of chips

Peripheral interface \ Product name		CMS32F0332GE32NA
MCU operating voltage		2.1V~5.5V
Maximum clock frequency		64MHz
Memory module	APROM	60/62/63/64KB (1)
	BOOT	0/1/2/4KB (1)
	Data FLASH	1KB
	SRAM	8KB
Timer	SysTick	1 (24-bit)
	WDT	1
	WWDT	1
	TIMER0/1/2/3	4 (16/32-bit)
Enhanced digital peripheral	CRC	CRC-16-CCITT
	DIVSQRT	32 bit/32 bit
	CCP	2
	EPWM	6(16-bit)
Communication interface	UART	2
	I2C	1
	SSP/SPI	1
Analog module	12bit-ADCA (number of external channels)	30
	12bit-ADCB (number of external channels)	30
	ACMP	2
	OP	2
	PGA	2
GPIOs		30
LVR		1.8V/2.0V/2.5V
LVD		2.0V/2.2V/2.4V/2.7V/3.0V/3.7V/4.0V/4.3V
Operating temperature		-40℃~85℃
Package		QFN32

Note: (1) Set the size of APROM and BOOT space through the system configuration register, and the maximum space of APROM and BOOT in total is 64KB.

(2) The number of analog modules and the analog functions are not implemented through pin inputs/outputs; the input/output pins are subject to the actual product.

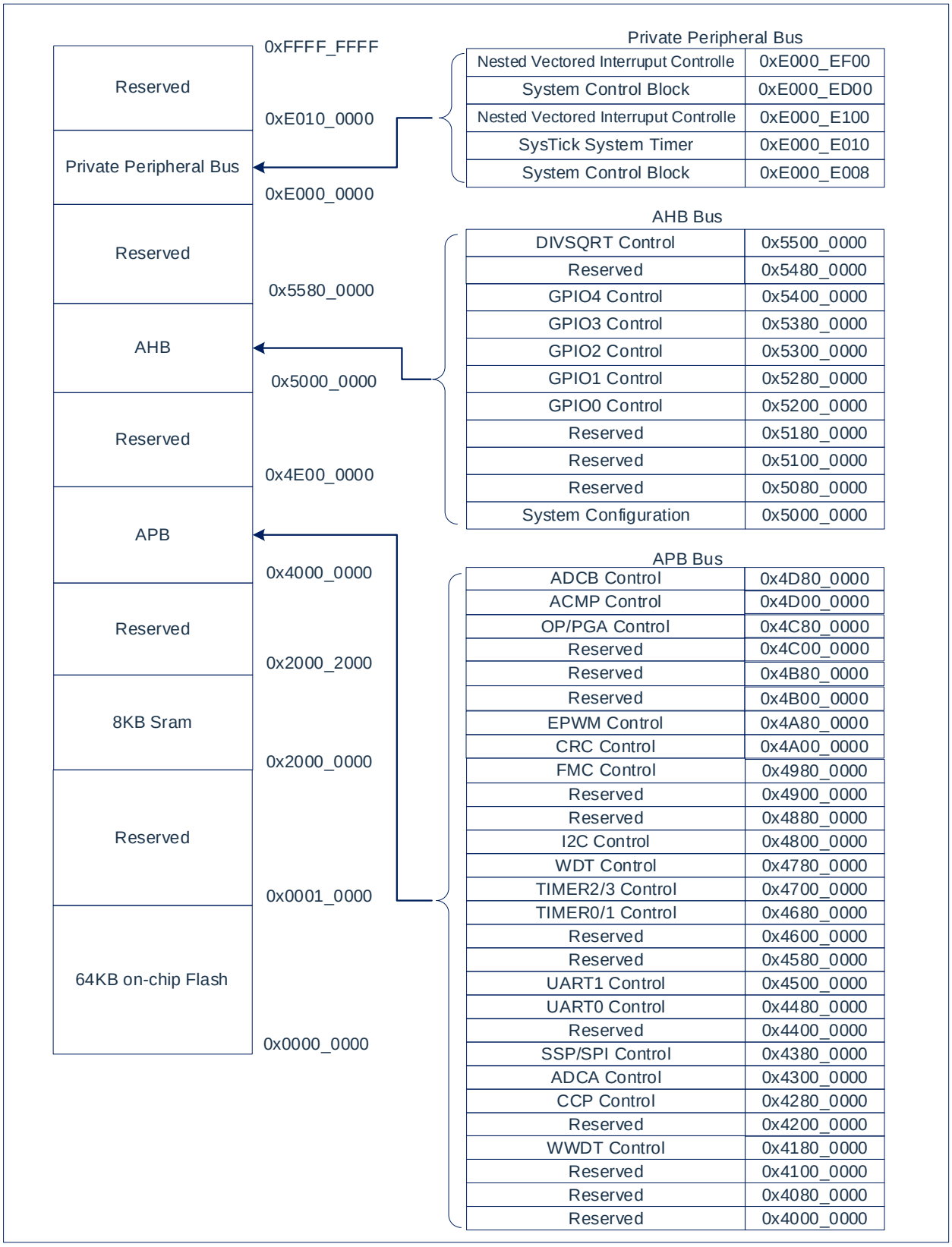
2. System Overview

2.1 Brief introduction

This series of products integrates an ARM® Cortex®-M0 core and a built-in Nested Vectored Interrupt Controller. Key features include parallel I/O ports (supporting general inputs, pull-up/pull-down inputs, push-pull outputs, open-drain outputs, with configurable edge or level-triggered interrupts), timers (6-bit windowed watchdog timer, 32-bit watchdog timer, 4 programmable timers), SPI, I2C, UART, PWM, CCP, ADC, ACMP, OPA, PGA, among other components. Main characteristics are as follows:

- Up to 64KB of FLASH memory, up to 8KB of SRAM, and a 1KB FLASH data area.
- Supports BOOT functionality, program space partition protection, hardware CRC for FLASH space codes, register protection operations, user-configurable ID for enhanced security.
- Supports normal mode, sleep mode, and deep sleep mode for convenience and lower power consumption.
- Features a 32-bit hardware divider, single-cycle 32-bit hardware multiplier for faster operations.
- Any IO port can be configured as a serial transmit and receive port, and any IO port can also be configured as an input port for ADC, which is more convenient to use.
- Features an enhanced PWM with period duty cycle interval updates and independent/complementary/synchronous/master control outputs.
- Includes a 12-bit ADC capable of up to 1.2Msps, analog IP such as analog comparators with hysteresis selection, programmable gain amplifiers with selectable gains, and operational amplifiers.

2.2 Memory mapping



Private Peripheral Bus

Nested Vectored Interruput Controlle	0xE000_EF00
System Control Block	0xE000_ED00
Nested Vectored Interruput Controlle	0xE000_E100
SysTick System Timer	0xE000_E010
System Control Block	0xE000_E008

AHB Bus

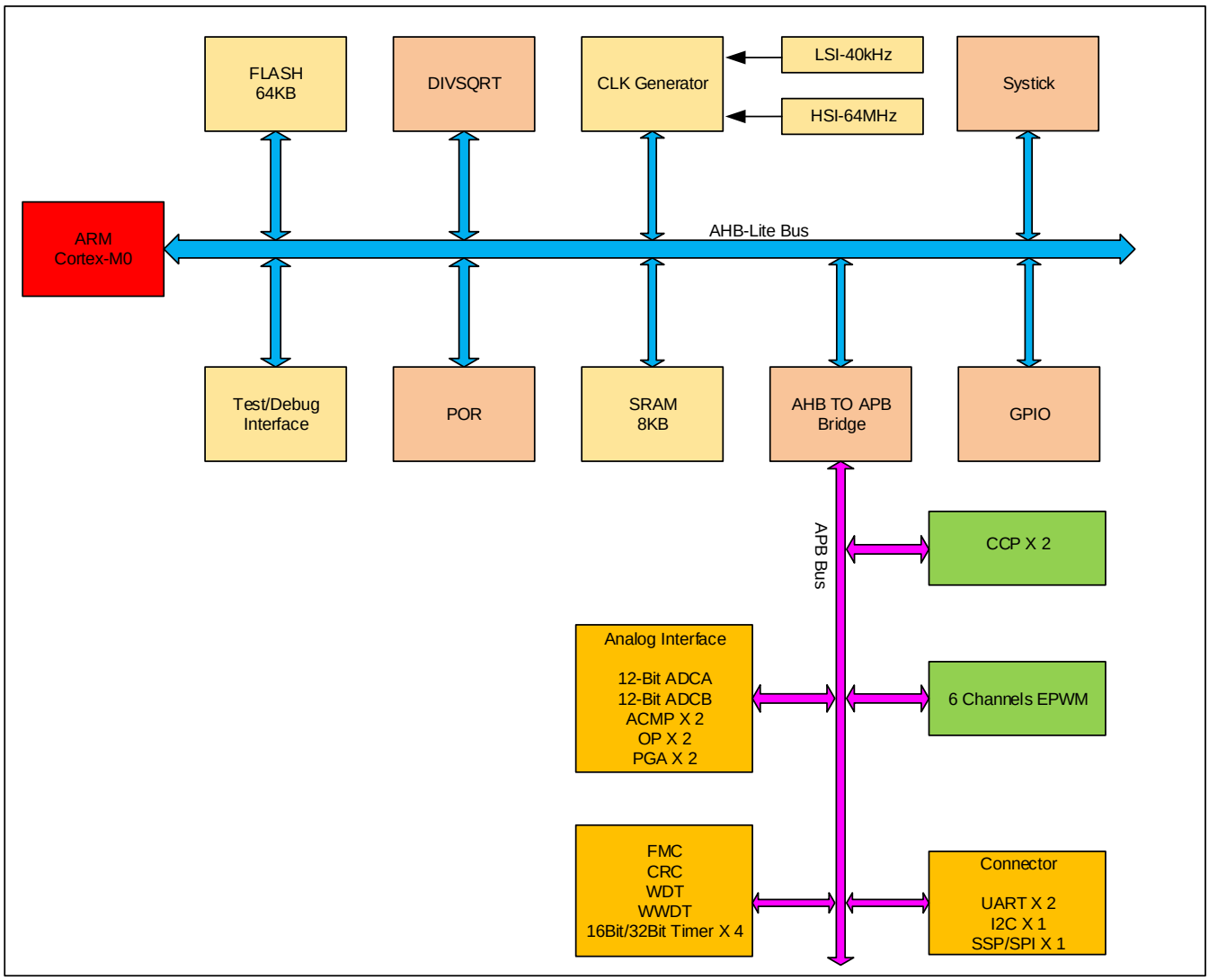
DIVSQRT Control	0x5500_0000
Reserved	0x5480_0000
GPIO4 Control	0x5400_0000
GPIO3 Control	0x5380_0000
GPIO2 Control	0x5300_0000
GPIO1 Control	0x5280_0000
GPIO0 Control	0x5200_0000
Reserved	0x5180_0000
Reserved	0x5100_0000
Reserved	0x5080_0000
System Configuration	0x5000_0000

APB Bus

ADCB Control	0x4D80_0000
ACMP Control	0x4D00_0000
OP/PGA Control	0x4C80_0000
Reserved	0x4C00_0000
Reserved	0x4B80_0000
Reserved	0x4B00_0000
EPWM Control	0x4A80_0000
CRC Control	0x4A00_0000
FMC Control	0x4980_0000
Reserved	0x4900_0000
Reserved	0x4880_0000
I2C Control	0x4800_0000
WDT Control	0x4780_0000
TIMER2/3 Control	0x4700_0000
TIMER0/1 Control	0x4680_0000
Reserved	0x4600_0000
Reserved	0x4580_0000
UART1 Control	0x4500_0000
UART0 Control	0x4480_0000
Reserved	0x4400_0000
SSP/SPI Control	0x4380_0000
ADCA Control	0x4300_0000
CCP Control	0x4280_0000
Reserved	0x4200_0000
WWDT Control	0x4180_0000
Reserved	0x4100_0000
Reserved	0x4080_0000
Reserved	0x4000_0000

2.3 Block diagram

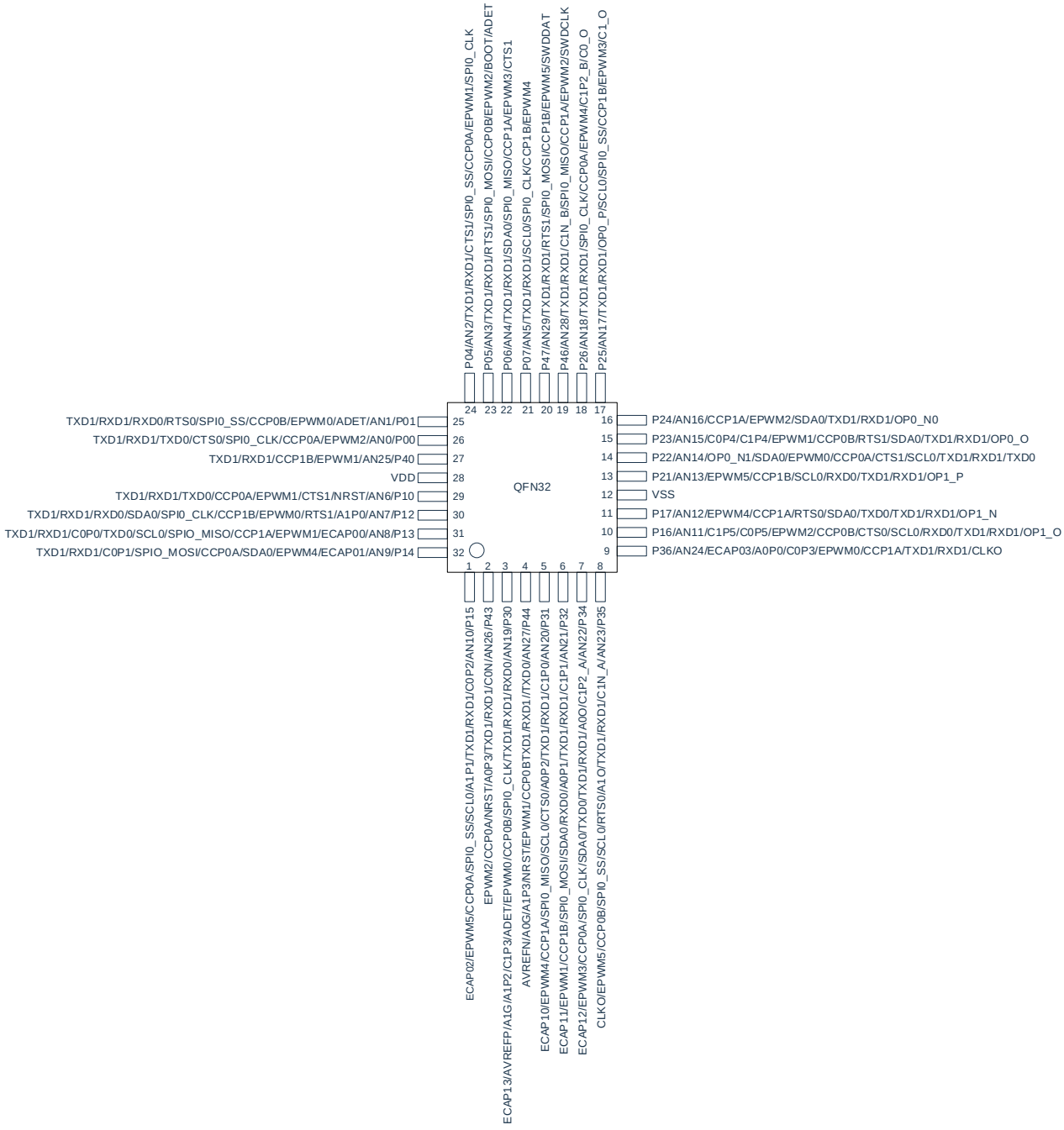
2.3.1 System architecture block diagram



3. Pin Definition

3.1 Pinouts

3.1.1 CMS32F0332GE32NA



Note: All pins in the pinout diagram can be mapped to TXD1 and RXD1 functions.

3.2 Analog function pins

Symbol	Description
C0P0	Comparator 0 positive input 0
C0P1	Comparator 0 positive input 1
C0P2	Comparator 0 positive input 2
C0P3	Comparator 0 positive input 3
C0P4	Comparator 0 positive input 4
C0P5	Comparator 0 positive input 5
C0N	Comparator 0 negative input
C1P0	Comparator 1 positive input 0
C1P1	Comparator 1 positive input 1
C1P2_A	Comparator 1 positive input 2_A
C1P2_B	Comparator 1 positive input 2_B
C1P3	Comparator 1 positive input 3
C1P4	Comparator 1 positive input 4
C1P5	Comparator 1 positive input 5
C1N_A	Comparator 1 negative input_A
C1N_B	Comparator 1 negative input_B
A0P0	PGA0 positive input 0
A0P1	PGA0 positive input 1
A0P2	PGA0 positive input 2
A0P3	PGA0 positive input 3
A0G	PGA0 pseudo-differential ground/op-amp mode negative input
A0O	PGA0 output/op-amp mode output
A1P0	PGA1 positive input 0
A1P1	PGA1 positive input 1
A1P2	PGA1 positive input 2
A1P3	PGA1 positive input 3
A1G	PGA1 pseudo-differential ground/op-amp mode negative input
A1O	PGA1 output/op-amp mode output
OP0_P	Op-amp 0 positive input
OP0_N0	Op-amp 0 negative input 0
OP0_N1	Op-amp 0 negative input 1
OP0_O	Op-amp 0 output
OP1_P	Op-amp 1 positive input
OP1_N	Op-amp 1 negative input
OP1_O	Op-amp 1 output
C0_O	Analog comparator 0 digital output
C1_O	Analog comparator 1 digital output
AVREFP	ADCB external reference positive
AVREFN	ADCB external reference negative

3.3 GPIO features

The pins share multiple functions, and each I/O port can be configured as a corresponding digital function or analog function. I/O as a general-purpose GPIO port has the following characteristics:

- It can be configured as a normal input, pull-up input, pull-down input, push-pull output, open-drain output mode without pull-up, and open-drain output mode with pull-up.
- It can be configured to a high level, low level, rising edge, falling edge, double edge trigger interrupt.
- It can be configured to a high level, low level, rising edge, falling edge to wake up the chip sleep/deep sleep mode.
- Configurable with 2 levels of I/O speed.
- Configurable with 2 levels of output current.

3.4 Pin function description

The symbols in the table below are described as follows.

Pin name	Description of symbol
I/O	Digital input/output.
I	Digital input.
O	Digital output.
AI	Analog input.
AO	Analog output.
P	Power or ground.

Pin No. QFN32	Pin name	Pin type	Description
1	P15	I/O	General purpose input/output pin
	AN10	AI	ADC analog input channel 10
	C0P2	AI	ACMP0 positive input channel 2
	ECAP02	I	ACMP0 positive input channel 2 as capture input
	A1P1	AI	PGA1 positive input channel 1
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	SCL0	I/O	I2C0 clock input/output pin
	SPI0_SS	I/O	SPI0 chip select pin
	CCP0A	I/O	CCP0 capture input/PWM output A-channel pin
	EPWM5	O	EPWM output channel 5
2	P43	I/O	General purpose input/output pin
	AN26	AI	ADC analog input channel 26
	C0N	AI	ACMP0 negative input channel
	A0P3	AI	PGA0 positive input channel 3
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	NRST	I	External reset pin
	CCP0A	I/O	CCP0 capture input/PWM output A-channel pin
	EPWM2	O	EPWM output channel 2
3	P30	I/O	General purpose input/output pin
	AN19	AI	ADC analog input channel 19
	AVREFP	AI	ADCB external reference positive

	C1P3	AI	ACMP1 positive input channel 3
	ECAP13	I	ACMP1 positive input channel 3 as capture input
	A1P2	AI	PGA1 positive input channel 2
	A1G	AI	PGA1 pseudo-differential ground/op-amp mode negative input
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	RXD0	I	UART0 data input pin
	SPI0_CLK	I/O	SPI0 clock input/output pin
	CCP0B	I/O	CCP0 capture input/PWM output B-channel pin
	EPWM0	O	EPWM output channel 0
	ADET	I	ADC external boot digital input
4	P44	I/O	General purpose input/output pin
	AN27	AI	ADC analog input channel 27
	AVREFN	AI	ADCB external reference negative
	A1P3	AI	PGA1 positive input channel 3
	A0G	AI	PGA0 pseudo-differential ground/op-amp mode negative input
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	NRST	I	External reset pin
	TXD0	O	UART0 data output pin
	CCP0B	I/O	CCP0 capture input/PWM output B-channel pin
	EPWM1	O	EPWM output channel 1
5	P31	I/O	General purpose input/output pin
	AN20	AI	ADC analog input channel 20
	C1P0	AI	ACMP1 positive input channel 0
	ECAP10	I	ACMP1 positive input channel 0 as capture input
	A0P2	AI	PGA0 positive input channel 2
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	CTS0	I	UART0 enable transmit pin
	SCL0	I/O	I2C0 clock input/output pin
	SPI0_MISO	I/O	SPI0 host input/slave output pin
	CCP1A	I/O	CCP1 capture input/PWM output A-channel pin
	EPWM4	O	EPWM output channel 4
6	P32	I/O	General purpose input/output pin
	AN21	AI	ADC analog input channel 21
	C1P1	AI	ACMP1 positive input channel 1
	ECAP11	I	ACMP1 positive input channel 1 as capture input
	A0P1	AI	PGA0 positive input channel 1
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	RXD0	I	UART0 data input pin
	SDA0	I/O	I2C0 data input/output pin
	SPI0_MOSI	I/O	SPI0 host output/slave input pin
	CCP1B	I/O	CCP1 capture input/PWM output B-channel pin
	EPWM1	O	EPWM output channel 1
7	P34	I/O	General purpose input/output pin
	AN22	AI	ADC analog input channel 22
	C1P2_A	AI	ACMP1 positive input channel 2

	ECAP12	I	ACMP1 positive input channel 2 as capture input
	A0O	AO	PGA0 output channel
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	TXD0	O	UART0 data output pin
	SDA0	I/O	I2C0 data input/output pin
	SPI0_CLK	I/O	SPI0 clock input/output pin
	CCP0A	I/O	CCP0 capture input/PWM output A-channel pin
	EPWM3	O	EPWM output channel 3
8	P35	I/O	General purpose input/output pin
	AN23	AI	ADC analog channel 23
	C1N_A	AI	ACMP1 negative input channel
	A1O	AO	PGA1 output channel
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	RTS0	O	UART0 request transmit pin
	SCL0	I/O	SPI0 clock input/output pin
	SPI0_SS	I/O	SPI0 chip select pin
	CCP0B	I/O	CCP0 capture input/PWM output B-channel pin
	EPWM5	O	EPWM output channel 5
	CLKO	O	System clock output pin
9	P36	I/O	General purpose input/output pin
	AN24	AI	ADC analog channel 24
	C0P3	AI	ACMP0 positive input channel 3
	ECAP03	I	ACMP0 positive input channel 3 as capture input
	A0P0	AI	PGA0 positive input channel 0
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	CCP1A	I/O	CCP1 capture input/PWM output A-channel pin
	EPWM0	O	EPWM output channel 0
	CLKO	O	System clock output pin
10	P16	I/O	General purpose input/output pin
	AN11	AI	ADC analog channel 11
	OP1_O	AO	OPA1 output channel
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	RXD0	I	UART0 data input pin
	SCL0	I/O	I2C0 clock input/output pin
	CTS0	I	UART0 enable transmit pin
	CCP0B	I/O	CCP0 capture input/PWM output B-channel pin
	EPWM2	O	EPWM output channel 2
	C1P5	AI	Comparator 1 positive input 5
	C0P5	AI	Comparator 0 positive input 5
11	P17	I/O	General purpose input/output pin
	AN12	AI	ADC analog channel 12
	OP1_N	AI	OPA1 negative input
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	TXD0	O	UART0 data output pin

	SDA0	I/O	I2C0 data input/output pin
	RTS0	O	UART0 request transmit pin
	CCP1A	I/O	CCP1 capture input/PWM output A-channel pin
	EPWM4	O	EPWM output channel 4
12	VSS	P	Ground
13	P21	I/O	General purpose input/output pin
	AN13	AI	ADC analog channel 13
	OP1_P	AI	OPA1 positive input
	ECAP11	I	ACMP1 positive input channel 1 as capture input
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	RXD0	I	UART0 data input pin
	SCL0	I/O	I2C0 clock input/output pin
	CCP1B	I/O	CCP1 capture input/PWM output B-channel pin
	EPWM5	O	EPWM output channel 5
14	P22	I/O	General purpose input/output pin
	AN14	AI	ADC analog channel 14
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	TXD0	O	UART0 data output pin
	SCL0	I/O	I2C0 clock input/output pin
	CTS1	I	UART1 enable transmit pin
	CCP0A	I/O	CCP0 capture input/PWM output A-channel pin
	EPWM0	O	EPWM output channel 0
	SDA0	I/O	I2C0 data input/output pin
	OP0_N1	AI	Op-amp 0 negative input 1
15	P23	I/O	General purpose input/output pin
	AN15	AI	ADC analog channel 15
	OP0_O	AO	OPA0 output channel
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	SDA0	I/O	I2C0 data input/output pin
	RTS1	O	UART1 request transmit pin
	CCP0B	I/O	CCP0 capture input/PWM output B-channel pin
	EPWM1	O	EPWM output channel 1
	C0P4	AI	Comparator 0 positive input 4
	C1P4	AI	Comparator 1 positive input 4
16	P24	I/O	General purpose input/output pin
	AN16	AI	ADC analog channel 16
	OP0_N0	AI	OPA0 negative input channel
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	SDA0	I/O	I2C0 data input/output pin
	ECAP03	I	ACMP0 positive input channel 3 capture input
	CCP1A	I/O	CCP1 capture input/PWM output A pin
	EPWM2	O	EPWM output channel 2
17	P25	I/O	General purpose input/output pin
	AN17	AI	ADC analog channel 17
	OP0_P	AI	OPA0 positive input channel
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin

	SCL0	I/O	I2C0 clock input/output pin
	SPI0_SS	I/O	SPI0 chip select pin
	CCP1B	I/O	CCP1 capture input/PWM output B-channel pin
	EPWM3	O	EPWM output channel 3
	C1_O	O	ACMP1 output channel
18	P26	I/O	General purpose input/output pin
	AN18	AI	ADC analog channel 18
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	SPI0_CLK	I/O	SPI0 clock input/output pin
	CCP0A	I/O	CCP0 capture input/PWM output A-channel pin
	EPWM4	O	EPWM output channel 4
	C0_O	O	ACMP0 output channel
	C1P2_B	AI	Comparator1 positive input 2
19	P46	I/O	General purpose input/output pin
	AN28	AI	ADC analog channel 28
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	SPI0_MISO	I/O	SPI0 host input/slave output pin
	C1N_B	AI	ACMP1 negative input channel
	CCP1A	I/O	CCP1 capture input/PWM output A channel pin
	EPWM2	O	EPWM output channel 2
	SWDCLK	I	SWD emulation clock input pin
20	P47	I/O	General purpose input/output pin
	AN29	AI	ADC analog channel 29
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	RTS1	O	UART1 request transmit pin
	SPI0_MOSI	I/O	SPI0 host output/slave input pin
	CCP1B	I/O	CCP1 capture input/PWM output B-channel pin
	EPWM5	O	EPWM output channel 5
	SWDDAT	I/O	SWD emulation data input/output pin
21	P07	I/O	General purpose input/output pin
	AN5	AI	ADC analog channel 5
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	SCL0	I/O	I2C0 clock input/output pin
	SPI0_CLK	I/O	SPI0 clock input/output pin
	CCP1B	I/O	CCP1 capture input/PWM output B-channel pin
	EPWM4	O	EPWM output channel 4
22	P06	I/O	General purpose input/output pin
	AN4	AI	ADC analog channel 4
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	SDA0	I/O	I2C0 data input/output pin
	SPI0_MISO	I/O	SPI0 host input/slave output pin
	CCP1A	I/O	CCP1 capture input/PWM output A-channel pin
	EPWM3	O	EPWM output channel 3
	CTS1	I	UART1 enable transmit pin
23	P05	I/O	General purpose input/output pin

	AN3	AI	ADC analog channel 3
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	RTS1	O	UART1 request transmit pin
	SPI0_MOSI	I/O	SPI0 host output/slave input pin
	CCP0B	I/O	CCP0 capture input/PWM output B-channel pin
	EPWM2	O	EPWM output channel 2
	BOOT	I	BOOT configuration input pin
	ADET	I	ADC external boot digital input
24	P04	I/O	General purpose input/output pin
	AN2	AI	ADC analog channel 2
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	CTS1	I	UART1 enable transmit pin
	SPI0_SS	I/O	SPI0 chip select pin
	CCP0A	I/O	CCP0 capture input/PWM output A-channel pin
	EPWM1	O	EPWM output channel 1
	SPI0_CLK	I/O	SPI0 clock input/output pin
25	P01	I/O	General purpose input/output pin
	AN1	AI	ADC analog channel 1
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	RXD0	I	UART0 data input pin
	RTS0	O	UART0 request transmit pin
	SPI0_SS	I/O	SPI0 chip select pin
	CCP0B	I/O	CCP0 capture input/PWM output B-channel pin
	EPWM0	O	EPWM output channel 0
	ADET	I	ADC external boot digital input
26	P00	I/O	General purpose input/output pin
	AN0	AI	ADC analog channel 0
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	TXD0	O	UART0 data output pin
	CTS0	I	UART0 enable transmit pin
	SPI0_CLK	I/O	SPI0 clock input/output pin
	CCP0A	I/O	PWM0 capture input/PWM output A-channel pin
	EPWM2	O	EPWM output channel 2
27	P40	I/O	General purpose input/output pin
	AN25	AI	ADC analog input channel 25
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	CCP1B	I/O	CCP1 capture input/PWM output B-channel pin
	EPWM1	O	EPWM output channel 1
-	VDD	P	Power supply
29	P10	I/O	General purpose input/output pin
	AN6	AI	ADC analog input channel 6
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	TXD0	O	UART0 data output pin

	NRST	I	External reset pin
	CCP0A	I/O	CCP0 capture input/PWM output A-channel pin
	EPWM1	O	EPWM output channel 1
	CTS1	I	UART1 enable transmit pin
30	P12	I/O	General purpose input/output pin
	AN7	AI	ADC analog input pin 7
	A1P0	AI	PGA1 positive input channel 0
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	RXD0	I	UART0 data input pin
	SDA0	I/O	I2C0 data input/output pin
	SPI0_CLK	I/O	SPI0 clock input/output pin
	CCP1B	I/O	CCP1 capture input/PWM output B-channel pin
	EPWM0	O	EPWM output channel 0
	RTS1	O	UART1 request transmit pin
31	P13	I/O	General purpose input/output pin
	AN8	AI	ADC analog input pin 8
	C0P0	AI	ACMP0 positive input channel 0
	ECAP00	I	ACMP0 positive input channel 0 as capture input.
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	TXD0	O	UART0 data output pin
	SCL0	I/O	I2C0 clock input/output pin
	SPI0_MISO	I/O	SPI0 host input/slave output pin
	CCP1A	I/O	CCP1 capture input/PWM output A-channel pin
	EPWM1	O	EPWM output channel 1
32	P14	I/O	General purpose input/output pin
	AN9	AI	ADC analog input pin 9
	C0P1	AI	ACMP0 positive input channel 1
	ECAP01	I	ACMP0 positive input channel 1 as capture input.
	TXD1	O	UART1 data output pin
	RXD1	I	UART1 data input pin
	SDA0	I/O	I2C0 data input/output pin
	SPI0_MOSI	I/O	SPI0 host output/slave input pin
	CCP0A	I/O	CCP0 capture input/PWM output A-channel pin
	EPWM4	O	EPWM output channel 4

3.5 Pin function list

Function symbol									
	CONFIG	0	1	2	3	4	5	6	7
P00		GPIO	ANA	TXD0	CTS0	SPI0_CLK	CCP0A	EPWM2	
P01		GPIO	ANA	RXD0	RTS0	SPI0_SS	CCP0B	EPWM0	ADET
P04		GPIO	ANA		CTS1	SPI0_SS	CCP0A	EPWM1	SPI0_CLK
P05	BOOT	GPIO	ANA		RTS1	SPI0_MOSI	CCP0B	EPWM2	ADET
P06		GPIO	ANA		SDA0	SPI0_MISO	CCP1A	EPWM3	CTS1
P07		GPIO	ANA		SCL0	SPI0_CLK	CCP1B	EPWM4	
P10	NRST	GPIO	ANA	TXD0			CCP0A	EPWM1	CTS1
P12		GPIO	ANA	RXD0	SDA0	SPI0_CLK	CCP1B	EPWM0	RTS1
P13		GPIO	ANA	TXD0	SCL0	SPI0_MISO	CCP1A	EPWM1	
P14		GPIO	ANA		SDA0	SPI0_MOSI	CCP0A	EPWM4	
P15		GPIO	ANA		SCL0	SPI0_SS	CCP0A	EPWM5	
P16		GPIO	ANA	RXD0	SCL0	CTS0	CCP0B	EPWM2	
P17		GPIO	ANA	TXD0	SDA0	RTS0	CCP1A	EPWM4	
P21		GPIO	ANA	RXD0	SCL0		CCP1B	EPWM5	
P22		GPIO	ANA	TXD0	SCL0	CTS1	CCP0A	EPWM0	SDA0
P23		GPIO	ANA		SDA0	RTS1	CCP0B	EPWM1	
P24		GPIO	ANA		SDA0		CCP1A	EPWM2	
P25		GPIO	ANA		SCL0	SPI0_SS	CCP1B	EPWM3	C1_O
P26		GPIO	ANA			SPI0_CLK	CCP0A	EPWM4	C0_O
P30		GPIO	ANA	RXD0		SPI0_CLK	CCP0B	EPWM0	ADET
P31		GPIO	ANA	CTS0	SCL0	SPI0_MISO	CCP1A	EPWM4	
P32		GPIO	ANA	RXD0	SDA0	SPI0_MOSI	CCP1B	EPWM1	
P34		GPIO	ANA	TXD0	SDA0	SPI0_CLK	CCP0A	EPWM3	
P35		GPIO	ANA	RTS0	SCL0	SPI0_SS	CCP0B	EPWM5	CLKO
P36		GPIO	ANA			CLKO	CCP1A	EPWM0	
P40		GPIO	ANA				CCP1B	EPWM1	
P43	NRST	GPIO	ANA				CCP0A	EPWM2	
P44	NRST	GPIO	ANA	TXD0			CCP0B	EPWM1	
P46		GPIO	ANA			SPI0_MISO	CCP1A	EPWM2	SWDCLK
P47		GPIO	ANA		RTS1	SPI0_MOSI	CCP1B	EPWM5	SWDDAT

Continued (TXD1 and RXD1 can be configured at any port)

Function symbol					Function symbol			
		8	9	GPIO	ANA (Multiple analog functions can be used simultaneously)			
PIN	Priority	UART1	UART1	ECAP	ADC	ACMP	PGA	OP
P00	Max	TXD1	RXD1		AN0			
P01					AN1			
P04					AN2			
P05					AN3			
P06					AN4			
P07					AN5			
P10					AN6			
P12					AN7		A1P0	
P13				ECAP00	AN8	C0P0		
P14	↓			ECAP01	AN9	C0P1		
P15				ECAP02	AN10	C0P2	A1P1	
P16					AN11	C1P5/C0P5		OP1_O
P17					AN12			OP1_N
P21					AN13			OP1_P
P22					AN14			OP0_N1
P23					AN15	C1P4/C0P4		OP0_O
P24					AN16			OP0_N0
P25					AN17			OP0_P
P26					AN18	C1P2_B		
P30				ECAP13	AN19/AVREFP	C1P3	A1P2/A1G	
P31				ECAP10	AN20	C1P0	A0P2	
P32	↓			ECAP11	AN21	C1P1	A0P1	
P34				ECAP12	AN22	C1P2_A	A0O	
P35					AN23	C1N_A	A1O	
P36				ECAP03	AN24	C0P3	A0P0	
P40					AN25			
P43					AN26	C0N	A0P3	
P44					AN27/AVREFN		A1P3/A0G	
P46	↓				AN28	C1N_B		
P47	min				AN29			

Note:

(1) When configured as 0, it is a GPIO function, and its input Schmitt is normally open (including when the state is output).

When configured as 1, all GPIO functions are closed, including the output circuit, Schmitt input circuit, and both pull-up and pull-down are closed.

(2) When configured as a digital function, the analog function can also be used. For example, when P13 is configured as a GPIO to use the ECAP function, the comparator C0P0 function can be used at the same time.

(3) The port supports the simultaneous use of multiple analog functions, such as the P25 can use the op amp function and the AD channel function at the same time.

(4) The SWD ports are fixedly configured as a group, which is set at the factory and cannot be modified by the user.

4. Function Summary

4.1 ARM Cortex–M0+ core

The Cortex®-M0 processor is a configurable 32-bit RISC processor with a multi-stage pipeline. It features an AMBA AHB-Lite interface and includes an NVIC component, along with optional hardware debugging capabilities. This processor executes Thumb instructions and is compatible with other Cortex®-M series processors. It supports two operational modes—Thread mode and Handler mode. When an exception occurs, the system enters Handler mode, and exception returns can only be executed in Handler mode. The system can enter Thread mode after reset and exception returns.

4.2 Memory

4.2.1 Program memory (FLASH)

The program memory is divided into two areas: APROM and BOOT, you can choose to boot from APROM or BOOT area when power is on.

Different product models have different program space sizes, depending on the specific model, the maximum space is 64KB.

The maximum space of BOOT is 4KB.

The BOOT size can be configured as follows:

64K (program storage area)				
Address space allocation method	APROM area		BOOT area	
Method 0	64K	0000H-FFFFH	-	-
Method 1	63K	0000H-FBFFH	1K	FC00H-FFFFH
Method 2	62K	0000H-F7FFH	2K	F800H-FFFFH
Method 3	60K	0000H-EFFFH	4K	F000H-FFFFH

4.2.2 Non-volatile data memory (Data FLASH)

Data FLASH has a space size of 1KB and is divided into two sectors. Each sector is write-protected. It can store the data that the user needs to save for power down.

4.2.3 Data memory (SRAM)

The maximum data memory is 8KB, and write protection can be set for every 2KB after the initial address.

4.3 Interrupt control

The Cortex®-M0 CPU provides a Nested Vector Interrupt Controller (NVIC) for interrupt handling with the following features:

- Support nested vector interrupts.
- Automatically save and restore processor state.
- Dynamically change priority.
- Simplify and define interruption time.

The system provides multiple peripheral interrupt sources, including GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, CCP, WWDT, EPWM, ADCA, ADCB, ACMP, UART0, UART1, TIMER0, TIMER1, TIMER2, TIMER3, WDT, I2C, SPI, SYS_CHK, the actual number of interrupt sources varies from product to product. Each interrupt supports 4 levels of interrupt priority, the highest priority is 0, the lowest priority is 3, and the default priority is 0.

4.4 Clock control

The clock controller provides the clock source for the entire chip, including the system clock and all peripheral clocks. The controller provides clock selection through separate clock switches, clock source selection and frequency dividers, as well as clock outputs through IO ports.

The clock source can be selected from the following two types:

- On-chip high-speed oscillator HIS (48MHz/64MHz).
- On-chip low-speed oscillator LSI (40KHz).

The clock output can be selected from the following two types:

- AHB bus clock AHBCLK.
- On-chip high-speed oscillator HSI.

4.5 Power management

4.5.1 Operating mode

The system has 3 different operating modes to suit the power requirements of different applications.

- Normal mode: MCU is in normal working mode, peripherals are running normally, LDO is turned on.
- Sleep mode: MCU is in sleep mode, CPU stops working, peripherals are running normally, LDO is turned on.
- Deep sleep mode: MCU is in deep sleep mode, CPU stops working, peripherals only work with WDT, and LDO is turned on.

4.5.2 Low voltage reset (LVR)

This series of products contains a low-voltage reset circuit, when the power supply voltage is lower than the set detection voltage, the system is reset.

There are 3 choices for low voltage detection voltage: 1.8V/2.0V/2.5V.

4.5.3 Low voltage detection (LVD)

This series of products contains a low-voltage detection circuit that can compare the power supply voltage with the set detection voltage. If the power supply voltage is lower than the set detection voltage, an interrupt request signal is generated.

There are 8 options for detection voltage: 4.3V/4.0V/3.7V/3.0V/2.7V/2.4V/2.2V/2.0V.

4.6 Timers

4.6.1 System timer (SysTick)

The Cortex®-M0 has a built-in system timer, SysTick, which provides a simple 24-bit write-clear, decrement counting, and auto-load initial value function, as well as a register with a flexible control mechanism. The counter can be used as a real-time operating system (RTOS) tick timer or as a simple timer peripheral.

4.6.2 Watchdog timer (WDT)

The watchdog timer is a 32-bit down counter with 40KHz as the counting clock source. When the system runs to an unknown state, the watchdog can be used to reset the system, thus avoiding the system from entering an infinite loop. The watchdog timer has the following characteristics:

- The counting clock can be selected from 1, 16, or 256 divisions.
- Support watchdog reset system.
- Support watchdog timer interrupts.
- Support watchdog interrupt to wake up the system in sleep/deep sleep mode.

4.6.3 Windowed watchdog timer (WWDT)

The windowed watchdog timer is a 6-bit down counter. The window watchdog timer is used to perform a system reset within a specific window time to prevent the program from going to an uncontrollable state under unpredictable conditions. The windowed watchdog timer has the following characteristics:

- 6-bit windowed comparison value can be set.
- Counting clock can choose 14 kinds of frequency division ratio.
- Support interrupt generation when the windowed watchdog count value is equal to the windowed comparison value.
- Support loading data when the windowed watchdog count value is greater than the windowed comparison value, generating a system reset.
- Support a system reset when the windowed count value is decremented to 0.

4.6.4 General timers (TIMER0/1/2/3)

This series of products includes 4 programmable 32-bit/16-bit down counters, which can provide users with convenient timing counting functions. TIMER0/TIMER1/ TIMER2/TIMER3 has the following characteristics:

- The counting clock can be selected from 1, 16, or 256 divisions.
- There are three counting operation modes: one-shot trigger, period counting, and continuous counting.
- Support delay load counting initial value function.
- Support generating an interrupt when the counter is decremented to 0.
- Support timer interrupt wake up sleep mode.

4.7 Enhanced digital peripherals

4.7.1 Cyclic redundancy check unit (CRC)

Cyclic Redundancy Check (CRC) is the most commonly used error-checking code in the field of data communication. Its distinctive feature is the ability to select arbitrary lengths for the information field and the checksum field. The CRC unit on the chip uses the polynomial "$X^{16}+X^{12}+X^5+1$" (CRC16-CCITT). By specifying the data to be checked through the program, this module is not limited to the code flash area and can be used for versatile checks.

4.7.2 Hardware divider (DIVSQRT)

This series of products includes a 32bit hardware divider, which has the following characteristics:

- Support unsigned or signed number division.
- With clear flag indication bit.
- The bit width of the quotient and remainder are both 32 bits.
- Write the divisor register to start the division operation.
- 16 HCLK clocks to complete an operation.

4.7.3 Capture/compare/pulse width modulation module (CCP0/1)

This series of products includes 2 groups of CCP modules (CCP0/CCP1), each group of CCP corresponds to A and B channels. CCP module supports PWM output, capture mode0, capture mode1 and interrupt.

(1) PWM output has the following characteristics:

- CCP0's A and B channels share one period register, while CCP1's A and B channels share another period register.
- CCP0/CCP1 A and B channels' duty cycles can be independently configured.
- Up to 4 PWM outputs are supported.
- Support 50% duty cycle square wave output.
- Output polarity is selectable.

(2) Capture mode0 has the following characteristics:

- CCP0 can select either channel A or B as the external capture input signal.
- CCP1 can select either channel A or B as the external capture input signal.
- Four capture modes are available: software start counting, capture on rising edge; software start counting, capture on falling edge; count on rising edge, capture on falling edge; count on falling edge, capture on rising edge.
- Capture condition triggers counter stop.

(3) Capture mode1 has the following characteristics:

- Only CCP1 has capture mode 1.
- CAP0, CAP1, CAP2, and CAP3: 4 capture channels, each with 4-bit control selecting different inputs.
- Software capture mode ca be triggerred by writing to registers.
- Edge capture mode can be triggered by external signals: rising edge, falling edge, both edges.
- Support CCP1 capture trigger CCP0 counter load enable.

(4) Capture mode 2 has the following characteristics.

- Only CCP1 has capture mode 2, CCP0 can be set freely.
- CAP1, CAP2, and CAP3 share the same capture channel for the same signal.
- Each channel can independently select the edge capture mode of rising edge, falling edge, and double edge triggering of external signals.
- CAP3 can automatically calculate the period and duty cycle data after the capture is completed.

(5) CCP module interrupt has the following characteristics:

- PWM interrupt.
- Capture mode 0 interrupt.
- CAP0, CAP1, CAP2, and CAP3 interrupts of capture mode 1.
- Counter overflow interrupt.

4.7.4 Enhanced PWM (EPWM)

The enhanced PWM module supports 6 PWM generators, and the period and duty cycle can be set independently. EPWM has the following characteristics:

- Support one-shot and continuous waveform outputs.
- Support 4 control modes: independent, complementary, synchronous, and group control.
- Counting clock can choose from 1, 2, 4, 8, or 16 frequency divisions.
- Support two counting modes: edge alignment and center alignment.
- Support 4 loading and update methods.
- Support output polarity selection.
- Support period, compare up, compare down, zero interrupts.

4.8 Communication module

4.8.1 Universal asynchronous receiver transmitter (UART0/1)

This series of products includes 2 full-duplex asynchronous communication interfaces, UART0 and UART1. The UART0/1 transceiver has the following characteristics:

- Full duplex, asynchronous communication.
- Register structure complies with 16550 industry standards.
- 16-byte transmit and receive FIFOs.
- Support hardware automatic flow control function (CTS, RTS).
- Support software flow control function (XOFF, XON).
- Support receive buffer trigger level selection.
- The data bit length can be set to 5~8 bits.
- The stop bit length can be set to 1, 1.5 or 2 bits.
- Generation and detection of parity, no parity or fixed parity bits can be set.

4.8.2 I^2C serial interface controller (I^2C)

This series of products includes a two-wire bidirectional serial bus controller I^2C. The I^2C controller has the following characteristics:

- Standard I^2C compatible bus interface.
- Support master/slave mode, two-way data transfer between master and slave.
- Support simultaneous data arbitration between multiple hosts to avoid serial data damage on the bus.
- The bus adopts serial synchronous clock, which can realize transmission between devices at different rates.
- Programmable clock can be used for multiple rate control.
- Support 7-bit/10-bit slave address mode.
- Support multi-address recognition.

4.8.3 Serial peripheral interface controller (SSP/SPI)

This series of products includes a synchronous serial controller SSP/SPI working in full-duplex mode. The SSP/SPI controller has the following characteristics:

- Compatible with Motorola's SPI, TI's 4-wire SSI and NS's Microwire bus.
- Support master or slave mode.
- Configurable transmit bit length.
- Configurable clock polarity and phase.
- Programmable clock rate control.
- Provide 8x 16-bit transmit/receive FIFOs.

4.9 Analog module

4.9.1 Analog-to-digital conversion (ADCA)

This series of products includes a 12-bit successive approximation analog-to-digital converter (ADC), which supports one-shot and continuous conversion modes. ADCA also has the following characteristics:

- Analog input voltage range: AVSS(VSS) ~ AVDD(VDD).
- Maximum sampling rate: 380Ksps.
- Up to 30 external single-ended analog input channels.
- Single conversion time: 21*T_{ADCK} (sampling time is 4 T_{ADCK}).
- One-shot mode: Perform an A/D conversion on the specified channel.
- Continuous mode: Perform A/D conversion on all selected channels.
- Support external input signal to trigger ADC conversion.
- Support interrupt generation after conversion.
- Built-in an AD conversion result comparator.
- The conversion result of each channel is stored in the corresponding data register.
- Channel 30 can test internal analog voltage signals (including OP0/1 outputs, PGA0/1 outputs, internal 1.2V reference voltage)

4.9.2 Fast analog-to-digital conversion (ADCB)

This series of products includes a 12-bit successive approximation analog-to-digital converter (ADCB), which supports one-shot and continuous conversion modes. ADCB also has the following characteristics:

- Analog input voltage range: AVSS(VSS/AVREFN) ~ AVDD(VDD/AVREFP).
- Maximum sampling rate: 1.2Msps.
- Up to 30 external single-ended analog input channels.
- Support two power consumption modes: high-speed mode and low-current mode.
- Single sampling and conversion time in high-speed mode: 52*T_{ADCK} (sampling time is set to 13.5*T_{ADCK}).
- One-shot mode: Perform an A/D conversion on the specified channel.
- Continuous mode: Perform A/D conversion on all selected channels.
- Support external input signal to trigger ADC conversion.
- Support interrupt generation after conversion.
- Built-in an AD conversion result comparator.
- The conversion result of each channel is stored in the corresponding data register.
- Channel 30 can test internal analog voltage signals (including OP0/1 outputs, PGA0/1 outputs, and internal 1.2V reference voltage).

4.9.3 Analog comparator (ACMP0/1)

This series of products contains 2 analog comparators, ACMP0 and ACMP1. ACMP0/1 has the following characteristics:

- Analog input voltage range: 0~(VDD-1.5V).
- Support hysteresis voltage selection (10mV/20mV/60mV- typical value).
- Positive can select multiple port inputs.
- Negative can select port input or internal reference voltage.
- A total of 16 selections for internal reference voltage division.

- Support output filtering, a total of 11 levels of filtering time can be selected.
- Interrupts are generated when the output changes from 0 to 1.

4.9.4 Operational amplifier (OP0/1)

This series of products includes 2 basic operational amplifier modules OP0 and OP1, and OP0/1 has the following characteristics:

- Can be configured in op-amp mode and comparator mode.
- Outputs can be measured by ADC.

4.9.5 Programmable gain amplifier (PGA0/1)

This series of products includes 2 programmable gain amplifiers, PGA0 and PGA1, and PGA0/1 has the following characteristics:

- Adjustable gains (4X/8X/10X/12X/14X/16X/32X).
- Support pseudo-differential inputs
- Support op-amp mode.
- Outputs can be measured by ADC.

4.10 Memory control module

FLASH memory includes program memory (APROM/BOOT) and non-volatile data memory (Data FLASH), which can be accessed through related special function registers (SFR) to realize IAP function. FLASH memory supports the following operations:

- Byte read operation.
- Byte write operation.
- Page erase operation.
- FLASH space CRC operation.

4.11 Safety function

4.11.1 Unique identification (UID)

Each chip has a 96-bit unique identification number, which has been set at the factory and cannot be modified by the user, but it can be read through the memory module.

4.11.2 User unique identification (USRUID)

This series of products features another 128-bit chip identification number called USRUID. It includes a user-settable 96-bit identification number and a fixed 32-bit identification number. This 128-bit identification code cannot be read via the memory module. USRUID can serve as a key in encryption applications, allowing user programs to establish protective mechanisms by detecting this key.

4.11.3 Program code protection

It supports code partition protection functionality, where each segment in the APROM space is 2KB and each segment in the BOOT space is 1KB. The protection status can be configured through user-configurable registers.

4.11.4 Data code protection

It supports data area protection function, where the data space is one segment per 0.5KB, and the protection status can be set through the user configuration registers.

4.11.5 Program CR

It supports hardware computation of program CRC check codes, with configurable check ranges. The CRC is generated using the polynomial CRC16-CCITT, defined as “$X^{16} + X^{12} + X^5 + 1$”.

4.11.6 General CRC calculation

The general CRC module can be used to verify the correctness of the program or data transmission. The check polynomial of the general CRC module is also generated using “$X^{16}+X^{12+}X^5+1$”.

4.11.7 Illegal memory access detection

If you access an illegal memory address in the ARM microcontroller, the bus system will respond with an error signal, which can provide a better method of program error detection.

4.11.8 SRAM protection function

The internal SRAM has a write protection function and can be set to partition write protection. Write protection does not affect the read function, the system register SRAMLOCK can set related functions.

4.11.9 SFR protection function

Some SFRs of key function modules have protection functions, and read and write operations are invalid in the protection state.

4.11.10 ADCA/B test function

Verify that the A/D converter is operating properly by performing A/D conversion on the positive reference voltage, negative reference voltage, analog input channel, and internal reference voltage of the A/D converter.

4.11.11 GPIO pin level detection

Regardless of whether the port is configured as an output port or an input port in GPIO function mode, the pin level can be read through GPIO->DI.

5. User Configuration

The user configuration area is a 128-word (512-byte) memory area allocated in FLASH, and the following functions can be set through the configuration area registers:

- LVR reset voltage.
- Power-on reset boot space (APROM/BOOT).
- User program, user UID, Data FLASH encryption control.
- Power-on WDT enable control, initial load value.
- SWD debugging function.
- External reset function and pin assignment.

6. Electrical Characteristics

Temperature condition is T_A = 25°C for the following parameters, unless otherwise indicated.

6.1 MCU absolute maximum ratings

Symbol	Item	Min.	Max.	Unit
V_{DD}-V_{SS}	Power supply voltage	-0.3	5.8	V
V_{IN}	Input voltage	V_{SS}-0.3	V_{DD}+0.3	V
T_A	Operating temperature	-40	85	℃
T_{ST}	Storage temperature	-55	150	℃
I_{DD}	V_{DD} maximum input current	-	120	mA
I_{SS}	V_{SS} maximum output current	-	120	mA
I_{IO}	Maximum sink current of a single I/O	-	50	mA
	Maximum source current of a single I/O	-	40	mA
	Maximum sink current of all I/Os	-	100	mA
	Maximum source current of all I/Os	-	100	mA

Caution: Operating the device beyond the "**Absolute Maximum Ratings**" range will cause permanent damage. Functionality is guaranteed only when the device operates within the specified range in the manual. Operating the chip under absolute maximum ratings conditions may affect the device's reliability.

6.2 MCU DC electrical parameters

(V_{DD}-V_{SS}=2.1~5.5V, T_A=25℃)

Symbol	Item	Test condition	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	HCLK=64MHz	2.1	-	5.5	V
I_{DD1}	Operating current	HCLK=64MHz, HSI=64MHz, ALL APBCLK OFF, V_{DD}=5.0V	-	6.5	-	mA
I_{DD2}		HCLK=64MHz, HSI=64MHz, ALL APBCLK OFF, V_{DD}=3.3V	-	6.5	-	mA
I_{DD3}		HCLK=48MHz, HSI=48MHz, ALL APBCLK OFF, V_{DD}=5.0V	-	5	-	mA
I_{DD4}		HCLK=48MHz, HSI=48MHz, ALL APBCLK OFF, V_{DD}=3.3V	-	5	-	mA
I_{DD5}		HCLK=40KHz, LSI=40KHz, ALL APBCLK OFF, V_{DD}=5V	-	0.25	-	mA
I_{DD6}		HCLK=40KHz, LSI=40KHz, ALL APBCLK OFF, V_{DD}=3.3V	-	0.25	-	mA
I_{DEEP_SLEEP}	Current in deep sleep mode	LDO ON, V_{DD}=5V	-	200	-	uA
		LDO in low power consumption mode, V_{DD}=5V	-	6	-	uA
V_{IL}	Input level, low	-	VSS	-	0.3VDD	V
V_{IH}	Input level, high	-	0.7VDD	-	VDD	V
I_{OL1}	Output current, low	V_{DD}=5V GPIOxDR[n]=0 V_{IO}=1.5V	-	-	50	mA
I_{OL2}	Output current, low	V_{DD}=5V GPIOxDR[n]=1 V_{IO}=1.5V	-	-	25	mA
I_{OH1}	Output current, high	V_{DD}=5V GPIOxDR[n]=0 V_{IO}=3.5V	-	-	40	mA
I_{OH2}	Output current, high	V_{DD}=5V GPIOxDR[n]=1 V_{IO}=3.5V	-	-	20	mA
R_{UP}	Pull-up resistance	-	-	33	-	KΩ
R_D	Pull-down resistance	-	-	33	-	KΩ
F_{AHBCLK}	AHB clock	-	-	-	64	MHz
F_{APBCLK}	APB clock	-	-	-	64	MHz

6.3 MCU AC electrical parameters

6.3.1 Power-on reset time

Symbol	Item	Test condition	Min.	Typ.	Max.	Unit
T_{RESET}	Reset time	V_{DD}=5V	-	6	-	ms
T_{VDDR}	V_{DD} rise rate	V_{DD}=5V	20	-	-	us/V
T_{VDDF}	V_{DD} fall rate	V_{DD}=5V	20	-	-	us/V

6.3.2 On-chip high-speed oscillator (HSI)

Symbol	Item	Min.	Typ.	Max.	Unit
V_{HSI}	Operating voltage	2.1	-	5.5	V
T_A	Operating temperature	-40	-	85	℃
I_{HSI}	Operating current, V_{DD}=5.0V,T_A=25℃	-	300	-	uA
F_{HSI48M}	T_A=25℃,V_{DD}=5.0V	-	48	-	MHz
	T_A=25℃,V_{DD}=2.1~5.5V	-1	-	1	%
	T_A=0℃~85℃,V_{DD}=2.1~5.5V	-2	-	2	%
	T_A= -40℃~85℃,V_{DD}=2.1~5.5V	-3	-	3	%
F_{HSI64M}	T_A=25℃,V_{DD}=5.0V	-	64	-	MHz
	T_A=25℃,V_{DD}=2.1~5.5V	-1	-	1	%
	T_A=0℃~85℃,V_{DD}=2.1~5.5V	-2	-	2	%
	T_A= -40℃~85℃,V_{DD}=2.1~5.5V	-3	-	3	%

6.3.3 On-chip low-speed oscillator (LSI)

Symbol	Item	Min.	Typ.	Max.	Unit
V_{LSI}	Operating voltage	2.1	-	5.5	V
T_A	Operating temperature	-40	-	85	℃
I_{LSI}	Operating current, V_{DD}=5.0V,T_A=25℃	-	10	-	uA
F_{LSI}	T_A=25℃, V_{DD}=5.0V	-	40	-	KHz
	T_A=25℃, V_{DD}=2.1~5.5V	-10	-	10	%
	T_A= -40℃~85℃, V_{DD}=2.1~5.5V	-15	-	15	%

6.3.4 Low voltage reset (LVR)

Symbol	Item	Min.	Typ.	Max.	Unit
V_{LVR1}	Low voltage detection threshold value: 1.8V	1.65	1.8	2.0	V
V_{LVR2}	Low voltage detection threshold value: 2.0V	1.85	2.0	2.2	V
V_{LVR3}	Low voltage detection threshold value: 2.5V	2.25	2.5	2.8	V

6.3.5 Low voltage detection (LVD)

Symbol	Item	Min.	Typ.	Max.	Unit
V_{LVD1}	Low voltage detection threshold value: 2.0V	1.85	2.0	2.15	V
V_{LVD2}	Low voltage detection threshold value: 2.2V	2.05	2.2	2.35	V
V_{LVD3}	Low voltage detection threshold value: 2.4V	2.25	2.4	2.55	V
V_{LVD4}	Low voltage detection threshold value: 2.7V	2.55	2.7	2.85	V
V_{LVD5}	Low voltage detection threshold value: 3.0V	2.85	3.0	3.15	V
V_{LVD6}	Low voltage detection threshold value: 3.7V	3.55	3.7	3.85	V
V_{LVD7}	Low voltage detection threshold value: 4.0V	3.85	4.0	4.15	V
V_{LVD8}	Low voltage detection threshold value: 4.3V	4.15	4.3	4.45	V

6.4 FLASH electrical parameters

Symbol	Item	Test condition	Min.	Typ.	Max.	Unit
V_F	FLASH operating voltage	-	2.1	-	5.5	V
T_F	FLASH operating temperature	-	-40	25	85	℃
$N_{ENDURANCE}$	Erase count	Program FLASH	20,000	-	-	Cycle
		Data FLASH	100,000	-	-	Cycle
T_{RET}	Data retention time	25℃	100	-	-	year
T_{ERASE}	Sector erase time	-	-	2.6	-	ms
T_{WRITE}	Write time	-	-	175	-	us
T_{READ}	Read time	-	-	4*Tsys	-	us
I_{DD1}	Read current	-	-	-	2.5	mA
I_{DD2}	Programming current	-	-	-	3.6	mA
I_{DD3}	Erase current	-	-	-	2	mA

Note: Tsys is the system clock period.

6.5 Analog circuit characteristics

6.5.1 BANDGAP electrical characteristics

Symbol	Item	Test condition	Min.	Typ.	Max.	Unit
V_{BG}	Internal reference 1.2V	V_{DD}=2.1~5.5V, T_A=25℃	1.188	1.2	1.212	V
		V_{DD}=2.1~5.5V, T_A= -40℃ to 85℃	1.182	1.2	1.218	V

Remark: Low-temperature specification values are guaranteed by design, and are not tested in mass production.

6.5.2 ADCA electrical characteristics

T_A=25℃.

Symbol	Item	Min.	Typ.	Max.	Unit
V_{AVDD}	ADC operating voltage	2.5	-	5.5	V
V_{REF}	Reference voltage	-	V_{AVDD}	-	V
V_{ADI}	Input voltage	0	-	V_{REF}	V
N_R	Resolution	12			Bit
DNL	Differential nonlinearity error (V_{REF}=V_{AVDD}=5V, T_{ADCK}=0.125us)	±2			LSB
INL	Integral nonlinearity error (V_{REF}=V_{AVDD}=5V, T_{ADCK}=0.125us)	±4			LSB
T_{ADCK}	ADC clock period	0.125	-	-	us
T_{ADC}	ADC conversion time (Sample hold time: 4*T_{ADC})	-	21	-	T_{ADCK}
F_S	Sampling rate (V_{REF}=V_{AVDD}=5V)	380			Ksps

6.5.3 ADCB electrical characteristics

T_A=25℃.

Symbol	Item	Min.	Typ.	Max.	Unit
V_{AVDD}	ADC operating voltage	2.5	-	5.5	V
V_{REF1}	Reference voltage 1	-	V_{AVDD}	-	V
V_{REF2}	Reference voltage 2 (positive AVREFP/negative AVREFN)	-	V_{AVREFP} V_{AVREFN}	-	V
V_{ADI}	Analog signal input	0	-	V_{REF}	V
N_R	Resolution	12			Bit
DNL	Differential nonlinearity error (T_{ADCK}=0.0156us, T_{ADC}=52*T_{ADCK}, V_{REF}=VDD)	±1.5			LSB
INL	Integral nonlinearity error (T_{ADCK}=0.0156us, T_{ADC}=52*T_{ADCK}, V_{REF}=VDD)	±2			LSB
T_{ADCK}	ADC clock period	0.0156	-	-	us
T_{ADC}	High-speed mode single AD sampling and conversion total time (sampling time=13.5*T_{ADCK})	-	52	-	T_{ADCK}
F_S	Sampling rate	1.2			Msps

Note: Quantization error is not included.

6.5.4 OP0/1 electrical parameters

T_A=25℃, V_{SENSE}=V_{IN+}-V_{IN-}, V_{DD}=5V, V_{IN+}=1V, unless otherwise indicated.

Symbol	Item	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Power supply voltage	-	2.5	-	5.5	V
I_Q	Quiescent current	V_{SENSE}=0mV	-	0.8	1.3	mA
I_{SD}	Shutdown current	-	-	10	-	nA
T_A	Operating temperature	-	-40	25	85	℃
Input characteristics						
V_{OS}	Input offset voltage	-	-8.0	±3.0	8.0	mV
V_{CM}	Common mode input voltage range	-40℃~85℃	0	-	V_{DD}-1.3	V
I_B	Input bias current	V_{SENSE}=0mV	-	10	-	pA
I_{OS}	Input offset current	V_{SENSE}=0mV	-	10	-	pA
Output characteristics						
C_{LOAD}	Capacitive load	-	-	30	-	pF
V_{OH}	Maximum output voltage	-40℃~85℃	-	-	V_{DD}-0.3	V
V_{OL}	Minimum output voltage	-40℃~85℃	0.3	-	-	V
Frequency characteristics						
A_{OL}	Open loop gain	-	-	80	-	dB
BW	Bandwidth	C_{LOAD}=30pF	-	5	-	MHz
PSRR	Power supply rejection ratio	V_{DD}=2.5~5.5V, V_{IN+}=1V, V_{SENSE}=0mV	-	70	-	dB
CMRR	Common mode rejection ratio	V_{IN+}=0.3~ (V_{DD}-1.5) -40℃~85℃	-	90	-	dB
Transient characteristics						
SR	Slew rate	R_{LOAD}=2K, C_{LOAD}=100pF	-	±7	-	V/μs
T_{STB}	Stable time	-	-	-	2	μs

Remark: This specification is guaranteed by the design, and is not tested in mass production.

6.5.5 ACMP0/1 electrical parameters

T_A=25℃, V_{SENSE}=V_{IN+}-V_{IN-}, V_{DD}=5V, V_{IN+}=1V, unless otherwise indicated.

Symbol	Item	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Power supply voltage	-	2.1	-	5.5	V
I_Q	Quiescent current	V_{SENSE}=0.1V	-	0.3	0.4	mA
I_{SD}	Shutdown current	V_{SENSE}=0.1V	-	5	-	nA
T_A	Operating temperature	-	-40	25	85	℃
Input characteristics						
V_{OS}	Input offset voltage	-	-10.0	±4.0	10.0	mV
V_{CM}	Common mode input voltage range	-40℃~85℃	-0.1	-	V_{DD}-1.3	V
I_B	Input bias current	V_{SENSE}=0mV	-	10	-	pA
I_{OS}	Input offset current	V_{SENSE}=0mV	-	10	-	pA
V_{HYS}	Input hysteresis voltage	V_{DD}=2.1~5.5V, V_{IN+}=0.5V	-	0 ±10 ±20 ±60	-	mV
Output characteristics						
V_{OH}	Maximum output voltage	-40℃~85℃	-	-	V_{DD}	V
V_{OL}	Minimum output voltage	-40℃~85℃	0	-	-	V
Frequency characteristics						
A_{OL}	Open loop gain	-	-	80	-	dB
BW	Bandwidth	-	-	120	-	MHz
PSRR	Power supply rejection ratio	V_{DD}=2.1~5.5V, V_{IN+}=1V, V_{SENSE}=0mV	-	80	-	dB
CMRR	Common mode rejection ratio	V_{DD}=2.1~5.5V, -40℃~85℃	-	90	-	dB
Transient characteristics						
T_{STB}	Stable time	-	-	-	2	μs
T_{PGD}	Response delay	V_{COM}=1V, V_{IN+}= V_{IN-} ±0.1V	-	50	100	ns

Remark: This specification is guaranteed by the design, and is not tested in mass production.

6.5.6 PGA0/1 electrical parameters

T_A=25℃, V_{DD}=5V, V_{IN+}=0.1V, unless otherwise indicated (G is the gain factor).

Symbol	Item	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Power supply voltage	-	2.5	-	5.5	V
I_Q	Quiescent current	V_{OUT}=2V	-	0.9	1.5	mA
I_{SD}	Shutdown current	-	-	10	-	nA
T_A	Operating temperature	-	-40	25	85	℃
Input characteristics						
V_{OS}	Input offset voltage	-	-8.0	±3.0	8.0	mV
V_{CM}	Common mode input voltage range	-40℃~85℃	0.35 /G	-	(V_{DD}-0.35)/ G	V
I_B	Input bias current	-	-	10	-	pA
I_{OS}	Input offset current	-	-	10	-	pA
Output characteristics						
EG	Gain error	G=4,8	-2	-	2	%
		G=10,12,14,16,32	-3	-	3	
C_{LOAD}	Capacitive load	-	-	10	-	pF
V_{OH}	Maximum output voltage	-40℃~85℃	-	V_{DD}-0.35	-	V
V_{OL}	Minimum output voltage	-40℃~85℃	-	0.35	-	V
V_{A0O} V_{A1O}	PGA0/1 test output ports (A0O, A1O)	-40℃~85℃ Output ports unloaded	-	-	V_{DD}-0.35	V
Frequency characteristics						
BW	Bandwidth	R_{LOAD}=2kΩ, C_{LOAD}=100pF G=4	-	2	-	MHz
PSRR	Power supply rejection ratio	V_{DD}=2.5~5.5V	-	60	-	dB
CMRR	Common mode rejection ratio	-40℃~85℃	-	80	-	dB
Transient characteristics						
SR	Slew rate	R_{LOAD}=2kΩ, C_{LOAD}=100pF G=4	-	7	-	V/μs
T_{STB}	Stable time	-	-	-	2	μs

Remark: This specification is guaranteed by the design, and is not tested in mass production.

6.6 EMC characteristics

6.6.1 EFT electrical characteristics

Symbol	Item	Test condition	Grade
V_{EFTB}	Fast transient voltage burst limits to beapplied through 0.1uF(capacitance) on VDDand VSSpins to induce a functional disturbance	T_A = + 25℃, HSI=64MHz, conforms to IEC 61000-4-4	4B

Note: The immunity performance against Electrical Fast Transient (EFT) pulses is closely related to system design aspects, including power supply structure, circuit design, layout and wiring, chip configuration, program structure, and more. The EFT parameters listed in the table are results obtained from testing on CMS internal testing platforms and may not apply universally to all application environments. These test data serve as reference only. Various aspects of system design can influence EFT performance. In applications where high EFT immunity is required, it is advisable to design while minimizing the impact of interference sources on system operation. It is recommended to analyze interference paths and optimize designs to achieve the best immunity performance against EFT disturbances.

6.6.2 ESD eletrical characteristics

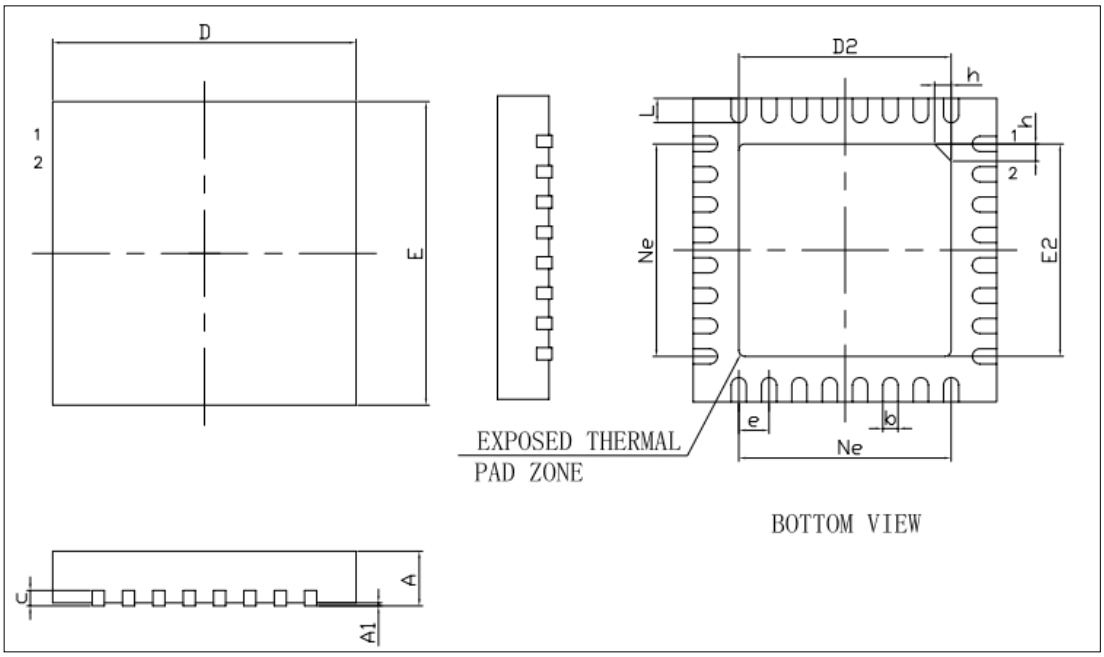
Symbol	Item	Test condition	Grade
V_{ESD}	Electrostatic discharge (Human-Body Model HBM)	T_A = + 25℃, JEDEC EIA/JESD22- A114	3A

6.6.3 Latch-Up eletrical characteristics

Symbol	Item	Test condition	Classification
LU	Static latch-up class	JEDEC STANDARD NO.78D NOVEMBER 2011	Class I (TA = +25℃)

7. Package Dimensions

7.1 QFN32（5x5x0.75-0.50mm）



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	-	3.75
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	-	3.75
L	0.30	-	0.45
h	0.30	0.35	0.40

Caution: Package dimensions do not include mold flash or gate burrs.

8. Ordering Information

Product No.	Core	Main frequency (MHz)	Program FLASH (KB)	Data FLASH (KB)	SRAM (KB)	Driver	LDO	Hardware multiplier	Hardware divider and square root unit	GPIO	12-Bit ADCA	12-Bit ADCB	Op-Amp	PGA	CMP	EPWM	CCP	Timer	UART	I2C	SPI	Temperature sensor	CRC	WDT	WWDT	PACKAGE
CMS32F0332 GE32NA	M0+	64	64	1	8	-	-	1	1	30	30	30	2	2	2	6	2	4	2	1	1	-	1	1	1	QFN32

9. Revision History

Version	Date	Description of changes
V0.5.0	January 2022	Initial version
V0.5.1	February 2023	Modified SWDCLK/SWDDAT function
V0.5.2	April 2023	1) Modified the operating temperature 2) Optimized the table content of 6.6 EMC characteristics. 3) Modified section 4.9.4.
V0.5.3	January 2024	Revised low voltage reset values in Section 1.1/1.2/4.5.2 and 6.3.4 Low voltage reset (LVR).
V0.5.4	May 2024	1) Modified the format of the pin map 2) Deleted the stop mode in 1.1. 3) Deleted the stop mode in 2.1. 4) Deleted the stop mode in 3.3. 5) Deleted the stop mode in 4.5.1. 6) Modified the table of electrical parameters in 6.2. 7) Modified the minimum value of common mode input voltage range in 6.5.6.
V0.5.5	September 2024	Revised the cover page
	October 2024	1) Modified the description of outages in Section 4.9.3 2) Modified QFN32 package dimensions